ABSTRACT

An apparatus and method provides efficient parallel processing for use with a single-bit sampler that provides single-bit samples at a high sample rate. A serial-to-parallel converter converts the single-bit samples into parallel single-bit samples at a reduced sample rate. A digital quadrature mix performs a frequency shift to the parallel single-bit samples and simultaneously performs a real-to-complex conversion of the parallel single-bit samples from the serial-to-parallel converter to provide parallel I and Q output values at an intermediate frequency. The serial-to-parallel converter has shift register stages that provide a memory for use in functional realization of a boxcar filter and decimation-by-two in the digital quadrature mix. The digital quadrature mix utilizes logic to route and invert the parallel single-bit samples resulting in the parallel I and Q single-bit output values. Additional filter and decimate stages may be used to process the parallel I and Q single-bit output values.